Yoshiaki KAWAI, S.N. 10/773,584 Page 2

## Amendments to the Specification

Please amend the paragraphs at page 2, lines 1-9, in the following manner:

## BACKGROUND OF THE INVENTION

## 1. Technical Field of the Invention

The present invention This disclosure generally relates to synchronization signal generators and, more particularly, to a synchronization signal generator, which generates a pixel clock for switching an image signal supplied to an optical beam modulator at delimitation of pixels, and an image forming apparatus using such a synchronization signal generator.

Please amend the paragraphs at page 2, line 11 through page 3, line 21, in the following manner:

There are known various methods for an image-forming process used in an image forming apparatus, which forms a color image according to electrophotography. Among those methods, there is a method that is referred to as a tandem type. In this method, a photo conductor and an image-forming process element are provided for each color component of a color image to be formed. The photo conductor and the image-forming process element are arranged along [[a]] an intermediate transfer member and a paper conveyance belt. Images formed in each color component are superimposed on the intermediate transfer member, and the superimposed full-color image is transferred onto a recording paper at once. Alternatively, a color image formed on each photo conductor is transferred onto a recording paper each time the recording paper, which is conveyed by the paper conveyance belt, passes through the transfer process part of each photo conductor so that a full color image is formed by causing the recording paper passes to pass through all transfer stations.

FIG. 1 shows a structure of a tandem type color image forming apparatus. In FIG. 1, photoconductor drums 6a-6d, which form images in different colors (yellow: Y/y, magenta: M/m, cyan: C/c, black: K/bk), are arranged in a single [|low]] row along a conveyance belt 10, which conveys a transfer paper (recording paper).

Yoshiaki KAWAI, S.N. 10/773,584 Page 3

According to an image signal for recording, laser beams modulated by image signals for Y, M, C and K recording are projected and scanned on the respective photoconductor drums 6a, 6b, 6c and 6d that have been charged uniformly by an electric charger so as to form electrostatic latent images thereon. Each electrostatic latent image is developed by respective Y, M, C, and K toner in respective developer 7a, 7b, 7c and 7d so as to form toner images (developed images: visible images) in each color.

Please amend the paragraphs at page 4, lines 5-10, in the following manner:

The transfer belt 10 is a transparent endless belt supported by a drive roller 9, a tension roller 13a and [[a]] an idle roller 13b. Since the tension roller 13a presses down the belt 10 with a spring (not shown in the figure), a tension applied to the belt 10 is substantially constant.

Please amend the paragraphs at page 10, line 6 through page 12, line 4, in the following manner:

## SUMMARY OF THE INVENTION

It is a general object of the present invention to provide an improved and useful synchronization signal generator and an image forming apparatus using such a synchronization signal generator in which the above mentioned problems are eliminated. A more specific object of the present invention is to provide In an aspect of this disclosure, there is provided a synchronization signal generator and an image forming apparatus using such a synchronization signal generator, which can easily generate a pixel clock that enables both a magnification correction in a main scanning direction and a correction of expansion and contraction of pixel width in the main scanning direction.

In order to achieve the above mentioned objects, there is provided according to one another aspect of the present invention this disclosure, there is provided a synchronization signal generator comprising [[:]] high-frequency clock generating means (40) for generating a high-frequency clock (PLLCLK) based on a reference

Dkt. 2271/71527

clock (REFCLK) and a synchronization detection signal (DETP\_N), [[;|] and a plurality of pixel clock generators each of which generates a clock signal (WCLK) based on the high-frequency clock signal and the synchronization detection signal (DETP\_N), wherein each of the pixel clock generators includes [[:]] pixel clock generating means (51) for dividing a frequency of the high-frequency clock (PLLCLK) so as to generate pulses of a reference period (0 dot), a long period (+1/8 dot) longer than the reference period and a short period (-1/8 dot) shorter than the reference period, and outputting, as a pixel clock (WCLK), one of the pulses that is designated by an output selection signal (PWMDAT), [[;]] first selection means (55) for outputting a first selection signal (PWM1), which selectively designates one of the pulses, in synchronization with the pixel clock (WCLK) in accordance with a timeseries distribution of the pulses of each period defined by a first set of data (A, B, C). [[;]] second selection means (56) for outputting a second selection signal (PWM2), which selectively designates one of the pulses, in synchronization with the pixel clock (WCLK) in accordance with a time-series distribution of the pulses of each period defined by a second set of data (A0-A3, B0-B3, C0-C3, D), [[;]] and synthesizing means (54) for synthesizing the first selection signal (PWM1) and the second selection signal (PWM2) so as to generate the output selection signal (PWMDAT) and output the output selection signal to the pixel clock generating means (51).

Please amend the paragraph at page 12, lines 10-18, in the following manner:

According to the above mentioned invention In a preferred embodiment, the designation of the output pulses according to the first selection signal (PWM1) changes in accordance with the time-series distribution of the pulses of each period defined by the first set of data (A, B, C). Thus, if the pulses are output as the pixel clock (WCLK) in accordance with the first selection signal (PWM1), a main-scanning magnification can be corrected by adjusting the first set of data (A, B, C).

Please amend the paragraphs at page 13, line 16 through page 15, line 11, in the following manner:

Yoshiaki KAWAI, S.N. 10/773,584 Page 5

> Additionally, there is provided according In another aspect of the present invention this disclosure, there is provided a synchronization signal generator comprising, in an exemplary embodiment, [[:]] high-frequency clock generating means (40) for generating a high-frequency clock (PLLCLK) based on a reference clock (REFCLK) and a synchronization detection signal (DETP\_N), [[;]] and a pixel clock generator that generates a clock signal (WCLK) based on the high-frequency clock signal and the synchronization detection signal (DETP\_N), wherein the pixel clock generator includes [[:]] pixel clock generating means (51) for dividing a frequency of the high-frequency clock (PLLCLK) so as to generate pulses of a reference period (0 dot), a long period (+1/8 dot) longer than the reference period and a short period (-1/8 dot) shorter than the reference period, and outputting, as the pixel clock (WCLK), one of the pulses that is designated by output selection data (PWMDAT), [[;]] first selection means (55) for outputting first selection data (PWM1), which selectively designates one of the pulses, in synchronization with the pixel clock (WCLK) in accordance with a time-series distribution of the pulses of each period defined by a first set of data (A, B, C), [[;]] second selection means (56) for outputting second selection data (PWM2), which selectively designates one of the pulses, in synchronization with the pixel clock (WCLK) in accordance with a timeseries distribution of the pulses of each period defined by a second set of data (A0-A3, B0-B3, C0-C3, D), [[;]] and synthesizing means (54) for adding the first selection signal (PWM1) and the second selection signal (PWM2) so as to generate the output selection data (PWMDAT) and output the output selection data to the pixel clock generating means (51).

According to the above mentioned In such embodiment of the present invention, since the synthesizing means (54) synthesizes the first selection data (PWM1) and the second selection data (PWM2) by summing them, there is no need to develop the first selection data (PWM1) and the second selection data (PWM2) on a line memory. Thus, a memory capacity can be saved, and the first selection data (PWM1) and the second selection data (PWM2), which are generated in a Raster mode (changes in time-series), can be synthesized in real time. Accordingly, reading and writing of the first selection data (PWM1) and the second selection data (PWM2)

Yoshiaki KAWAI, S.N. 10/773,584 Page 6

with respect to a memory can be omitted, which simplifies the signal processing.

Please amend the paragraph at page 16, line 8 through page 18, line 6, in the following manner:

Additionally, there is provided according to In another aspect of the present this disclosure, there is provided a synchronization signal generator comprising [[:]] high-frequency clock generating means (40) for generating a highfrequency clock (PLLCLK), [[;]] and a pixel clock generator, wherein the pixel clock generator includes [[:]] pixel clock generating means (51) for dividing a frequency of the high-frequency clock (PLLCLK) so as to generate pulses of a reference period (0 dot), a long period (+1/8 dot) longer than the reference period and a short period (-1/8 dot) shorter than the reference period, and outputting, as a pixel clock (WCLK), one of the pulses that is designated by output selection data first selection means (55) for outputting first selection data (PWMDAT), [[;]] (PWM1), which selectively designates one of the pulses, in synchronization with the pixel clock (WCLK) in accordance with a time-series distribution of the pulses of each period defined by a first set of data (A, B, C), [[:]] second selection means (56) for outputting second selection data (PWM2), which selectively designates one of the pulses, in synchronization with the pixel clock (WCLK) in accordance with a timeseries distribution of the pulses of each period defined by a second set of data (A0-A3, B0-B3, C0-C3, D), [[;]] and synthesizing means (54) for synthesizing the first selection data (PWM1) and the second selection data (PWM2) so as to generate the output selection data (PWMDAT), wherein values of the data designating the pluses of the reference period (0 dot), the long period (+1/8 dot) longer than the reference period and the short period (-1/8 dot) shorter than the reference period are set to numerical values a, b and c, respectively, and wherein the synthesizing means (54) sets the output selection data (PWMDAT) to the value a(0) when both the first selection data (PWM1) and the second selection data (PWM2) are a, and sets to the value b when one of the first selection data (PWM1) and the second selection data (PWM2) is a and the other is b. [1;]] the synthesizing means (54) sets the output

Yoshiaki KAWAI, S.N. 10/773,584 Page 7

selection data (PWMDAT) to the value b and carries over a remainder b to a following pixel when both the first selection data (PWM1) and the second selection data (PWM2) are b, and sets to the value a when one of the first selection data (PWM1) and the second selection data (PWM2) is b and the other is  $c_{\star}$  [[;]] and the synthesizing means (54) sets the output selection data (PWMDAT) to the value c and carries over a remainder c to a following pixel when both the first selection data (PWM1) and the second selection data (PWM2) are c.

Please amend the paragraphs at page 18, line 25 through page 20, line 8, in the following manner:

Additionally, there is provided according to In another aspect of the present invention there is provided an image forming apparatus comprising [[:]] charging means for electrically charging a plurality of photoconductors (6a-6d), [[;]] synchronization signal generator (135), according to one of claims 1, 5 and 8; optical modulation means (31y, 31m, 31c, 31bk) for switching image signals for image forming of each color in synchronization with each pixel clock (K\_, M\_, C\_, Y\_WCLK) generated by each clock generator (51, 53bk, 53m, 53c, 53y) of the synchronization signal generator (135), and radiating light beams corresponding to the image signals, [[;]] an exposure optical system (5) that projects and scans the light beams on the respective photoconductors, [[;]] developing means (7a-7d) for developing a latent image on each of the photoconductors with each color toner to form visible images of each color, [[;]] transfer means (10, 11a-11d) for transferring the visible images on a transfer sheet in an overlapping state, [[;]] front end synchronization detection means (38y, 38m, 38c, 38bk) for detecting each light beam for each color image forming projected on a front end of each main-scanning line for each color image forming so as to generate a end detection signal for each mainscanning line, [[;]] rear end synchronization detection means (40y, 40m, 40c, 40bk) for detecting each light beam for each color image forming projected on a rear end of each main-scanning line for each color image forming so as to generate a rear end detection signal for each main-scanning line, [[;]] and main-scanning magnification

Yoshiaki KAWAI, S.N. 10/773,584 Page 8

correction means (131) for measuring an interval from the front end detection signal to the rear end detection signal for at lest one color, and operating the first set of data (A, B, C) addressed to each color in accordance with a measured value of the interval.

According to the above mentioned invention. The effects the same as obtained with the above-mentioned synchronization signal generators according to the above mentioned invention can also be obtained in the image forming apparatus.

Please amend the paragraphs at page 20, line 18 through page 26, line 3, in the following manner:

In the image forming apparatus according to the present invention a preferred embodiment, the reference period (0 dot), the long period (+1/8 dot) and the short period (-1/8 dot) are generated by dividing the frequency of the high-frequency clock (PLLCLK). Accordingly, since the length of the main-scanning line and the variation of the pixel-width are adjusted based on differences in period between the three kinds of pulses, the interval can be measured based on the same unit of measurement as the differences in period. Thereby, the length of the main-scanning line and the distribution of variation of the pixel-width can be accurately adjusted, which results in an accurate main-scanning magnification correction and an accurate pixel-width variation correction.

In the image forming apparatus according to the present invention preferred embodiment, the main-scanning magnification correction means (131) may adjust the frequency (M, N) of the high-frequency clock (PLLCLK) so that the measurement value with respect to the light beam of a reference color (bk) matches a reference value, and the main-scanning magnification correction means (131) also adjusts a number (A) of pixels to which the pulses of the long period (+1/8 dot) or the short period (-1/8 dot) contained in the first set of data (A, B, C) and an interval of insertion.

According to the above-mentioned invention preferred embodiment, the pixel clock used for the reference color (bk) is set to be a reference main-scanning

Dkt. 2271/71527

rnagnification by adjustments of the frequency (M. N) of the high-frequency clock (PLLCLK) as a unit of pulse period. On the other hand, the pixel clocks used for other colors are set to be the reference main-scanning magnification by an operation applied to the first set of data (A, B, C). Thereby, the main-scanning magnification is matched to the reference design value, and the main-scanning magnification of other colors is matched to the main-scanning magnification of the reference color (bk). In this case, since setting value of PLL is changed for adjustment of the frequency (M, N) of the high-frequency clock (PLLCLK), it needs a certain time until the PLL becomes stable, that is a considerable time is spent on the main-scanning magnification correction. However, according to the present-invention preferred embodiment, the fundamental period of the pixel clock can be the reference design value by which the main-scanning magnification is determined.

In the image forming apparatus according to the present invention preferred embodiment, when the main-scanning magnification correction between pages is specified, in the main-scanning magnification correction, the main-scanning magnification correction means (131) may adjust a number (A) of pixels to which the pulses of the long period (+1/8 dot) or the short period (-1/8 dot) contained in the first set of data (A, B, C) and an interval of insertion with respect to the light beams for each color in accordance with a difference between the measured valued and the reference value.

According to the above-mentioned invention preferred embodiment, the main-scanning magnification of each color is matched individually to the reference design value. In this case, since the frequency (M, N) of the high-frequency clock (PLLCLK) is not adjusted, the fundamental period of the pixel clock shifts from the reference design value. Therefore, the main-scanning magnification may be matched to the reference value by adjusting the number of pulses (C) of the long period (+1/8 dot) or the short period (-1/8 dot), which may result in a variation of the pixel width in its entirety. However, such a variation is extremely small in practice. Since the setting of PLL is not changed, the main-scanning magnification correction is completed in a short time. Thus, there is only a small decrease in productivity when a continuous printing is performed with the main-scanning magnification correction

T-824 P.011/040 F-365

Yoshiaki KAWAI, S.N. 10/773,584 Page 10

applied between pages.

Additionally, there is provided according to In another aspect of the present invention this disclosure, an image forming apparatus comprising [[:]] modulation means (31y, 31m, 31c, 31bk) for modulating each of light beams emitted from a front end synchronization detection means (38y, plurality of light sources, [[;]] 38m; 38c, 38bk) for generating a synchronization signal providing a reference for a main-scanning line, [[:]] and rear end synchronization detection means (40y, 40m; 40c, 40bk) for detecting a position of a rear end of one line, wherein an image is formed on a photoconductor by irradiating the light beams onto the photoconductor through a scanner optical system, and a main-scanning magnification correction is performed according to a result of measurement of an interval between a front end synchronization detection signal (PSYNCN) and a rear end synchronization detection signal (PSYNCN), the image forming apparatus further comprising [[:]] highfrequency clock generation means (40) common to the plurality of light beams for generating a high-frequency clock (PLLCLK), which corresponds to a setting value, from a reference clock, wherein the high-frequency clock generation means (40) includes [[:]] pixel clock generation means (51y, 51m, 51c, 51bk) for generating one of a reference period, a short period shorter than the reference period and a long period longer than the reference period on an individual pixel basis by dividing a frequency of the high-frequency clock, [[;]] and pixel clock control means (53y, 53m, 53c, 53bk) for controlling designation information (a number of pixels that do not have the reference period, an interval of insertion of the pixel) to the pixel clock generation means on an individual pixel basis, wherein the pixel clock control means includes [[:]] a first control unit (a magnification error correction unit 55y, 55m, 55c, 55bk) that corrects the pixel clock in accordance with a result of measurement (A, B, C) of an interval between the front end synchronization detection signal and the rear end synchronization detection signal so as to correct a magnification error in one line, a second control unit (pixel-width variation correction unit 56y, 56m, 56c, [[:]]56bk) that corrects the pixel clock in accordance with expansion and contraction distortion data (A0-A3, B0-B3, C0-C3) previously acquired so as to correct an expansion and contraction distortion due to characteristics of the optical system, [[;]]

T-824 P.012/040 F-365

Yoshiaki KAWAI, S.N. 10/773,584 Page 11

> and a pixel clock correction data synthesizing unit (54y, 54m, 54c, 54bk) that synthesizes main-scanning magnification correction data and pixel-width variation correction data (PWM1[1:0], PWM2[1:0]), wherein a color offset between each color is corrected by adjusting the number of pixels that do not have the reference period and the interval of insertion of the pixels.

> According to the above-mentioned invention image forming apparatus, since the common PLL is shared by the pixel clock generation units of the plurality of light beams, the main-scanning magnification error correction can be achieved at a low cost. Moreover, since the pixel clock is generated based on the pixel clock correction data, which is obtained by synthesizing the magnification error correction data and the magnification difference correction data, an image having less color offset can be formed.

Please amend the paragraphs at page 26, line 24 through page 33, line 22, in the following manner:

> There is provided according to In another aspect of the present invention this disclosure, there is provided a method of generating a synchronization signal, comprising [[:]] generating a high-frequency clock (PLLCLK) based on a reference clock (REFCLK) and a synchronization detection signal (DETP\_N), [[:]]dividing a frequency of the high-frequency clock (PLLCLK) so as to generate pulses of a reference period (0 dot), a long period (+1/8 dot) longer than the reference period and a short period (-1/8 dot) shorter than the reference period, and outputting, as a pixel clock (WCLK), one of the pulses that is designated by an output selection generating a first selection signal (PWM1), which signal (PWMDAT), [[;]] selectively designates one of the pulses, in synchronization with the pixel clock (WCLK) in accordance with a time-series distribution of the pulses of each period defined by a first set of data (A, B, C), [[;]] generating a second selection signal (PWM2), which selectively designates one of the pulses, in synchronization with the pixel clock (WCLK) in accordance with a time-series distribution of the pulses of each period defined by a second set of data (A0-A3, B0-B3, C0-C3, D), [[;]]

Yoshiaki KAWAI, S.N. 10/773,584 Page 12

synthesizing the first selection signal (PWM1) and the second selection signal (PWM2) so as to generate the output selection signal (PWMDAT). [[;]] and generating the synchronization signal (PSYCN\_N) in accordance with the pixel clock (WCLK) and the synchronization detection signal (DETP\_N).

Additionally, there is provided according to In another aspect of the present invention this disclosure, there is provided a method of generating a synchronization signal, comprising [[:|] generating a high-frequency clock (PLLCLK) based on a reference clock (REFCLK) and a synchronization detection signal (DETP\_N), [[;]] dividing a frequency of the high-frequency clock (PLLCLK) so as to generate pulses of a reference period (0 dot), a long period (+1/8 dot) longer than the reference period and a short period (-1/8 dot) shorter than the reference period, and outputting, as the pixel clock (WCLK), one of the pulses that is designated by output selection data generating first selection data (PWM1), which selectively (PWMDAT), [[;]] designates one of the pulses, in synchronization with the pixel clock (WCLK) in accordance with a time-series distribution of the pulses of each period defined by a first set of data (A, B, C), [[;]] generating second selection data (PWM2), which selectively designates one of the pulses, in synchronization with the pixel clock (WCLK) in accordance with a time-series distribution of the pulses of each period defined by a second set of data (A0-A3, B0-B3, C0-C3, D), [[;]] summing the first selection signal (PWM1) and the second selection signal (PWM2) so as 10 generate and output the output selection data (PWMDAT), [[;]] and generating the synchronization signal (PSYCN\_N) in accordance with the pixel clock (WCLK) and the synchronization detection signal (DETP\_N).

There is provided according to In another aspect of the present invention this disclosure, there is provided a method of generating a synchronization signal, comprising [[:]] generating a high-frequency clock (PLLCLK) based on a reference clock (REFCLK) and a synchronization detection signal (DETP\_N). [[:]] dividing a frequency of the high-frequency clock (PLLCLK) so as to generate pulses of a reference period (0 dot), a long period (+1/8 dot) longer than the reference period and a short period (-1/8 dot) shorter than the reference period, and outputting, as a pixel clock (WCLK), one of the pulses that is designated by output selection data

Dkt. 2271/71527

generating first selection data (PWM1), which selectively (PWMDAT), [[;]] designates one of the pulses, in synchronization with the pixel clock (WCLK) in accordance with a time-series distribution of the pulses of each period defined by a first set of data (A, B, C), [[;]] generating second selection data (PWM2), which selectively designates one of the pulses, in synchronization with the pixel clock (WCLK) in accordance with a time-series distribution of the pulses of each period defined by a second set of data (A0-A3, B0-B3, C0-C3, D), [[;]] synthesizing the tīrst selection data (PWM1) and the second selection data (PWM2) so as to generate the output selection data (PWMDAT), and generating the synchronization signal (PSYCN\_N) in accordance with the pixel clock (WCLK) and the synchronization detection signal (DETP\_N), wherein values of the data designating the pluses of the reference period (0 dot), the long period (+1/8 dot) longer than the reference period and the short period (-1/8 dot) shorter than the reference period are set to numerical values a, b and c, respectively, and wherein the step of synthesizing includes [[:]] setting the output selection data (PWMDAT) to the value a when both the first selection data (PWM1) and the second selection data (PWM2) are a, and sets to the value b when one of the first selection data (PWM1) and the second selection data (PWM2) is a and the other is b. [[;]] setting the output selection data (PWMDAT) to the value b and carries over a remainder b(1) to a following pixel when both the first selection data (PWM1) and the second selection data (PWM2) are b, and sets to the value a when one of the first selection data (PWM1) and the second selection data (PWM2) is b and the other is c<sub>2</sub> [[;]] and setting the output selection data (PWMDAT) to the value c and carries over a remainder c to a following pixel when both the first selection data (PWM1) and the second selection data (PWM2) are c.

Further, there is provided according to In another aspect of the present invention this disclosure, there is provided a method of forming an image, comprising [[:]] electrically charging a plurality of photoconductors (6a-6d), [[:]] generating a line synchronization signal according to the above-mentioned method of forming an image, [[:]] switching image signals for image forming of each color in synchronization with each pixel clock (K\_, M\_, C\_, Y\_WCLK), and radiating light beams corresponding to the image signals, [[:]] projecting and scanning the light

Yoshiaki KAWAI, S.N. 10/773,584 Page 14

beams on the respective photoconductors, [[;]] developing a latent image on each of the photoconductors with each color toner to form visible images of each color, [[;]] transferring the visible images on a transfer sheet in an overlapping state, [[;]] detecting each light beam for each color image forming projected on a front end of each main-scanning line for each color image forming so as to generate a front end detection signal for each main-scanning line, [[;]] detecting each light beam for each color image forming projected on a rear end of each main-scanning line for each color image forming so as to generate a rear end detection signal for each main-scanning line, [[;]] and measuring an interval from the front end detection signal to the rear end detection signal for at lest one color, and operating the first set of data (A, B, C) addressed to each color in accordance with a measured value of the interval.

Additionally, there is provided according to In another aspect of the present this disclosure, there is provided a method of forming an image, avention comprising [[:]] modulating each of light beams emitted from a plurality of light sources, [[;]] generating a synchronization signal providing a reference for a mainscanning line, [[;]] and detecting a position of a rear end of one line, wherein an image is formed on a photoconductor by irradiating the light beams onto the photoconductor through a scanner optical system, and a main-scanning magnification correction is performed according to a result of measurement of an interval between a front end synchronization detection signal (PSYNCN) and a rear end synchronization detection signal (PSYNCN), the method further comprising [[:]] generating a highfrequency clock (PLLCLK), which corresponds to a setting value, from a reference clock, generating one of a reference period, a short period shorter than the reference period and a long period longer than the reference period on an individual pixel basis by dividing a frequency of the high-frequency clock, [[;]] controlling designation information (a number of pixels that do not have the reference period, an interval of insertion of the pixel) to the pixel clock generation means on an individual pixel basis, [[;]] correcting the pixel clock in accordance with a result of measurement (A, B, C) of an interval between the front end synchronization detection signal and the rear end synchronization detection signal so as to correct a magnification error in one line, [[;]] correcting the pixel clock in accordance with expansion and contraction

Dkt. 2271/71527

distortion data (A0-A3, B0-B3, C0-C3) previously acquired so as to correct an expansion and contraction distortion due to characteristics of the optical system, [[;]] synthesizing main-scanning magnification correction data and pixel-width variation correction data (PWM1[1:0], PWM2[1:0]), [[;]] and correcting a color offset between each color is corrected by adjusting the number of pixels that do not have the reference period and the interval of insertion of the pixels.

Other objects aspects, features and advantages of the present invention will become more apparent from the following detailed description when read in conjunction with the accompanying drawings.